Remarks

In the Office Action of August 26, 2005, the Examiner rejected claims 1, 2, 4-6, and 15-19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,927,130 to Suzuki ("Suzuki") in view of U.S. Patent No. 6,395,589 to Yu ("Yu"). For the following reasons, Applicants respectfully traverse these rejections.

Claim 1 is directed to a semiconductor FinFET device comprising an insulator; a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device; a source region formed at a first end of the semiconductor layer, a height of the source region being higher than that of the fin; a drain region formed at a second end of the semiconductor layer, a height of the drain region being higher than that of the fin; a metal gate region formed to overlap at a top surface and at least one side surface of the fin; and oxide sidewalls formed adjacent to the metal gate region and above the top surface of the fin.

Applicants submit that Suzuki and Yu, either alone or in combination, do not disclose or suggest each of the features recited in claim 1. For example, neither Suzuki nor Yu discloses or suggests a semiconductor FinFET device including a fin portion corresponding to a channel of the semiconductor device and a metal gate region formed to overlap at a top surface and at least one side

surface of the fin.

More specifically, neither Suzuki nor Yu discloses or suggests a "fin portion corresponding to a channel of the semiconductor device," as recited in claim 1. A "fin," as described in the specification and as is well known in the art, refers to a vertical conducting channel in a FinFET type of MOSFET (see, for example, the pending specification, paragraph 0026).

Suzuki does not disclose a fin portion corresponding to a channel of the semiconductor device, as recited in claim 1. Suzuki is directed to the manufacture of a trench gate type field effect transistor. (Suzuki, Title). The transistor of Suzuki is not a FinFET. Instead, the channel region of Suzuki, as with a traditional MOSFET, appears to be located entirely below the gate structure of the MOSFET. This can be seen in Figs. 1I and 2I of Suzuki, in which the portion of impurity layer 13 below gate structure G appears to be the channel region of the FET of Suzuki.

The FinFET device recited in claim 1 also includes a metal gate region formed to overlap at a top surface and at least one side surface of the fin. By overlapping at a top surface and at least one side surface of the fin, a vertical conducting channel may be formed to create the FinFET device. As mentioned in the previous paragraph, gate G of Suzuki appears to be located above the channel region. Accordingly, in Suzuki, there is no structure corresponding to the fin recited in claim 1 and certainly the gate of Suzuki does not overlap a fin at a

top surface and at least one side surface. The formation of the gate G in Suzuki is described, for example, at column 6, lines 17-28, and column 7, lines 22-27. As described in these sections, a trench is formed in the silicon substrate, which is then filled with a gate material. The trench appears to be formed in a single etching step that does not include formation of any additional structure that could be used to overlap "at a top surface and at least one side surface" of a fin, as required by claim 1.

The Examiner appears to be relying on Yu to disclose the insulator recited in claim 1. Yu, however, does not cure the above noted deficiencies of Suzuki. That is, Yu, as with Suzuki, does not disclose a fin portion corresponding to a channel of a semiconductor device, as recited in claim 1. Yu is directed to the fabrication of a fully depleted field effect transistor. (Yu, Title). The transistor of Yu is not a FinFET. Instead, the channel region of Yu, as with a traditional MOSFET, appears to be located entirely below the gate structure of the MOSFET. This can be clearly seen in Fig. 17 of Yu, in which gate structure 246 is positioned above a thin silicon channel region.

Yu also does not disclose or suggest "a metal gate region formed to overlap at a top surface and at least one side surface of the fin," as required by claim 1. As mentioned, Yu does not disclose a fin. Further, even if the channel region below gate structure 246 was somehow construed to correspond to a fin, the gate structure 246 of Yu does not overlap at a top surface and at least one

side surface of the fin. Instead, gate structure 246 appears to only cover a top surface of the underlying channel area.

For at least these reasons, Applicants submit that Suzuki and Yu, even if combined as the Examiner suggests, do not disclose or suggest each of the features recited in claim 1. Accordingly, the rejection of claim 1 based on Suzuki and Yu is improper and should be withdrawn. The rejection of claims 2, 4-6, and 19 based on Suzuki and Yu are also improper and should be withdrawn, at least by virtue of the dependency of these claims from claim 1.

Claims 2, 4-6, and 19 recite additional features that are not disclosed or suggested by Suzuki and Yu. Claim 2, for example, recites that the "metal gate region overlaps the top surface and two side surfaces of the fin." (emphasis added). The Examiner states that Fig. 2J of Suzuki discloses this feature of claim 2. (Office Action, page 4). Applicants respectfully disagree with the Examiner's interpretation of Suzuki. In Fig. 2J of Suzuki, a channel region between the source S and drain D regions appears to extend only below gate G. Nowhere does Suzuki disclose or suggest that the gate in some way "wraps" around the channel portion of the device. Accordingly, Suzuki cannot be said to disclose or suggest a metal gate region that overlaps a top surface and two side surfaces of a fin, as recited in claim 2.

Independent claim 15 and its dependent claims 16-18 also stand rejected under 35 U.S.C. § 103(a) based on Suzuki and Yu. For the following reasons,

Applicants respectfully traverse this rejection.

Claim 15 is directed to a FinFET device including an insulator and a semiconductor layer formed on the insulator. The semiconductor layer includes a fin portion corresponding to a channel of the semiconductor device. The FinFET device further includes a source region formed from a first end of the semiconductor layer, a height of the source region being higher than that of the fin and a width of the source region being wider than that of the fin. Further, the FinFET device includes a drain region formed from a second end of the semiconductor layer, a height of the drain region being higher than that of the fin and a width of the drain region being wider than that of the fin. The FinFET device also includes a metal gate region formed to overlap at a top surface and at least one side surface of the fin and sidewalls spacers formed adjacent at least portions of the metal gate region.

Claim 15 includes a number of features similar to those in claim 1. For instance, claim 15 recites "a fin portion corresponding to a channel of the semiconductor device" and "a metal gate region formed to overlap at a top surface and at least one side surface of the fin." For reasons similar to those given above with regard to claim 1, Applicants submit that the rejection of claim 15 based on Suzuki and Yu are also improper and should be withdrawn. More specifically, neither Suzuki nor Yu disclose the fin or the metal gate region recited in claim 15. Thus, even if combined as the Examiner suggests, Suzuki and Yu

would still not disclose each of the features recited in claim 15.

Claim 15 additionally recites a source and a drain region, in which a height and a width of the source and drain regions are higher and wider, respectively, than that of the fin. The Examiner states that a height of the source region S and the drain region D of Suzuki is higher than that of the fin, (Office Action, sentences bridging pages 5 and 6), but does not address the feature of claim 15 relating to the width of the source and drain region. In fact, Applicants submit that in Suzuki, because the source and drain regions are formed from a single substrate 1, in which a trench is made to create source region S, drain region D, and the channel (which the Examiner contends corresponds to the fin recited in claim 15), the source region S and drain region D of Suzuki appear to have the same width as the channel, and thus could not be said to be wider than the channel.

For at least these reasons, Applicants submit that Suzuki and Yu, even if combined as the Examiner suggests, do not disclose or suggest each of the features recited in claim 15. Accordingly, the rejection of this claim should be withdrawn. Claims 16-18 depend from claim 15 and the rejections of these claims are also improper and should be withdrawn.

In view of the foregoing remarks, Applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
Brian Ledell
Reg. No. 42,784

Date: November 22, 2005
11240 Waples Mill Road
Suite 300
Fairfax, VA 22030
Telephone: (571) 432-0800
Facsimile: (571) 432-0808